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Public Authority for Applied Education & Training

College of Technical Studies

Electronics Engineering Department

مختبر الكترونيات

Electronics I

ENT134

Lab Manual

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Experiment No. (1)
Diode Characteristics

Objectives:

To demonstrate FORWARD and REVERSE current and voltage characteristics of a "p n" junction diode.

Theoretical Background:

As forward current (I_F) through a diode increases, forward voltage (V_F) across does the same. However due to the changing characteristics of the forward biased diode, V_F will increase at much lower rate than I_F. When a diode is reverse biased, the reverse current (I_R) through the device will be extremely low, even when there is a significant reverse voltage (V_R) across the diode. This is due to the extremely high resistance of reverse biased diode.

Materials and equipment:

1- Power Supply.
2- AVO meter (analog).
1- Small signal Diode.
1- Rectifier Diode.
1- Resistor 1 kΩ.

Procedure:

1- Identify the terminals of the diode.

2- Use the AVO meter to measure the forward resistance of the diodes, and record in Table (1.1).

Diode number	Forward Resistance	Reverse Resistance

Table (1.1)

3- Reverse the diodes and measure the reverse resistance, and record in Table (1.1).

3- Set the circuit of Figure (1.1).

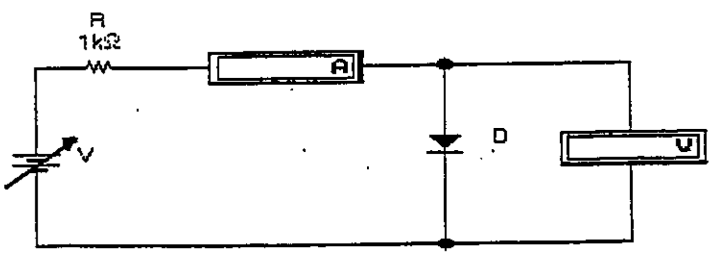


Fig (1.1)

4- Increase the voltage so that you have forward current as indicated in Table (1.2), and record the voltage

Forward current(mA)	Forward voltage (v).
0	0
0.5	
1.0	
1.5	
2.0	
3.0	
4.0	
5.0	
6.0	
7.0	
8.0	

Table (1.2)

5- Repeat for all other currents, and complete Table (1.2).

6- Reverse polarity of the diode as shown in Figure (1.2).

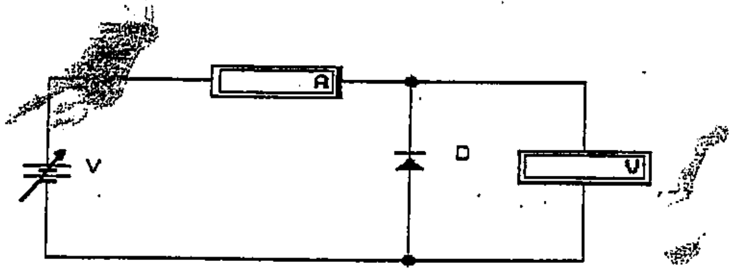


Figure 1.2.

7- Increase the reverse voltage as indicated in table (1.3), measure and record reverse current.

Reverse Current (μA)	Reverse Voltage(V)
	1
	5
	10
	20
	30
	40

Table 1.3

8- Using the data you collected in Tables (1.2) and (1.3), plot the points that represents each reading, compare your curve with the one you studied in the lecture.

9- Calculate the forward, and reverse resistance R_F, R_R using the equation
$R = \Delta V / \Delta I$

10-Discuss in your own words, what you have observed, concluded from this experiment.

Experiment No. (2)
Half-Wave Rectifier

Objective:

To demons[illegible] construction, and operation of half-wave rectifier.

Theoretical Background:

The half-wave rectifier is the simplest of the rectifier circuits .It converts ac input to pulsating dc by simply eliminating either the positive alternations of the input (for a negative dc power supply), or the negative alternations of the input (for a positive dc power supply).

Materials and equipment:

1-Oscilloscope
1-AVO meter (analog).
1-Transformer, rated 240 V_{ac} input and 12 V_{ac} output.
1- Si Rectifier Diode (# 547).
1- Resistor 5.6 kΩ.
(225)

Part I (Experimental)

Procedure:

1- Construct the circuit of Figure (2.1).

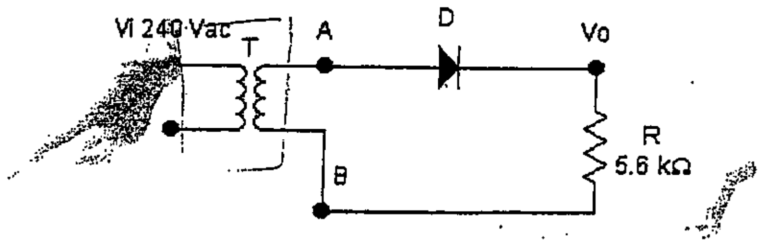


Fig (2.1)

2- Apply power to the circuit.

3- Measure and record the rms and peak-to-peak voltage as indicated in Table (2.1).

4- To calculate the input and output frequencies, measure the input and output time period, record in Table (2.1).

Points	AVO meter	Oscilloscope			
******	******	Number of squares	V/Div. T/Div.	Result	Wave-form
V_{AB}					
V_o					
T_{in}	******* ***** ******* ***** ******* *****				f = 1/T
T_o	******* ***** ******* ***** ******* ****				f =1/T

Table 2.1

5- Reverse the diode, an[illegible] the output waveform.

Part II (Computer Simulation)
Procedure:

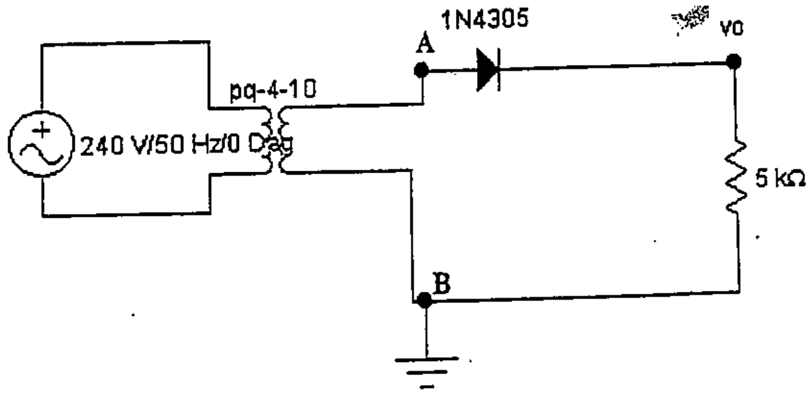


Fig (2.2)

1- Setup the circuit of Figure 2.2 using (Electronics Workbench Software).
2- Connect the oscilloscope to the input terminals AB, and the output terminals Vo.
3- Observe the signal waveforms, and print out, to submit with your report.

Report

1- Is $V_{AB(rms)}$ measured = $\frac{V_{AB(p)}}{\sqrt{2}}$

2- Is the value of $V_{O(dc)}$ measured = 0.318 V_P?

3- What is the PIV for the diode used?

4- Write brief conclusion about the main idea of the experiment.

Experiment No. (3)
Full-Wave Bridge Rectifier

Objective:

To demonstrate the construction, and operation of center-tapped transformer full-wave rectifier.

Theoretical Background:

The full-wave center-tapped rectifier changes ac to pulsating dc by either converting the negative alternations to positive alternations (for positive dc power supply) or by converting the positive alternations of input signal to negative alternations (for a negative dc power supply).

Materials and Equipment:

1-Oscilloscope.
1-AVO-meter (analog).
1-Transformer, rated 240 V_{ac} input and 12 V_{ac} output (614)
2-Si Rectifier Diode (#547).
1-Resistor 5.6 kΩ

Part I (Experimental)
Procedure:

1- Construct the circuit of Figure (3.1).

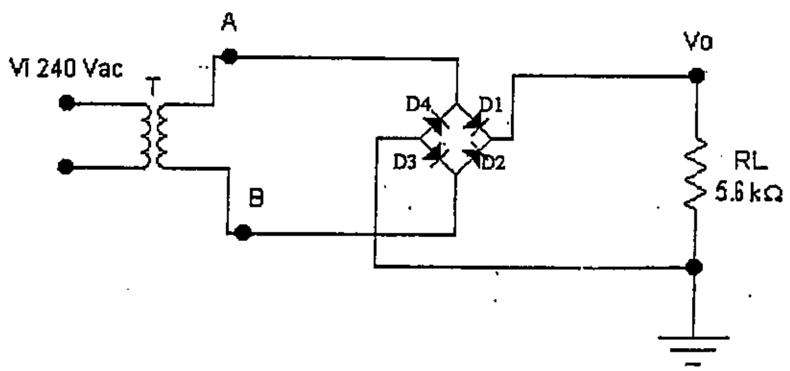


Figure 3.1

2- Apply power to the circuit.

3- Measure the rms and peak to peak values of the secondary voltage of the transformer V_{AB} record in Table 3.1.

4- Measure the output voltage Vo as indicated in Table 3.1.

5- Remove the load resistor R_L from the circuit, measure and observe the waveform at point Vo record in Table 3.1.

6- Disconnect power from the circuit and return R_L to its original position in the circuit. Now, remove D_1 from the circuit and apply power.

7- Observe and measure the output waveform, record in Table 3.1.

8- Measure the time period of the input and output signal.

Points	AVO meter	Oscilloscope			
******	******	Number of squares	V/Div. T/Div.	Result	Wave-form
V_{AB}					
V_O					
Vo No Load R_L					
Vo One Diode Removed					
T_{in}	******* ******* ******* ******* **				f = 1/T
T_o	******* ***** ******* ***** ******* ****				f = 1/T

Table 3.1

Part II (Computer Simulation)
Procedure:

1- Setup the circuit of Figure 3.2 using (Electronics Workbench Software).

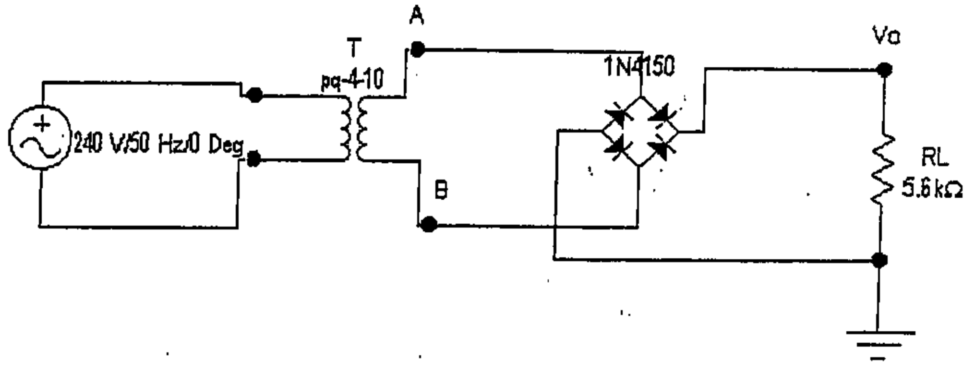


Fig 3.2

2- Connect channel 1 of the oscilloscope to the secondary terminals of the transformer A.B observe the waveform.

3- Connect channel 2 of the oscilloscope to the output of the rectifier circuit observe the waveform.

Report:

1- Explain why an open load resistor caused the waveform you saw in step 5 of the practical procedure.
2- Explain why an open diode in the bridge caused the waveform you saw in step.6 of the practical procedure.
3- Is the value of $V_{O(dc)} = 0.638\ V_P$?
4- What should be the PIV for the diodes used in the experiment?
5- Write brief conclusion about the main idea of the experiment.
6- Submit a printout of the waveforms in the simulation procedure.

Experiment No. (4)
Zener Diode

Objectives:

- To demonstrate the constant-voltage characteristics of the Zener diode.
- To introduce zener diode as voltage regulator.
-

Theoretical Background:

The zener diode is a component that maintains a relatively constant voltage across its terminals even when there is a relatively large change in device current. The voltage across the terminals is a approximately equal to the nominal **Zener voltage (V_z)** of the component as long as the device current stays within a specified range. The typical tolerance in terminal voltage is ± 20 %.

A constant dc output voltage is what we seek from regulated power supplies, to do this a zener is used to adjust it self from variation of input source or load resistance which causes the change in voltage level .

Materials and Equipment:

1-Power supply.
1-AVO-meter (analog).
1-Resistor 100 Ω.
1-Zener diode(# 531) .
1- Resistor 500 Ω.
1- Digital voltmeter.
1- Resistor Box.

Part A (Zener Diode Characteristics)

Procedure:

1- Construct the circuit shown in Figure (4.1).

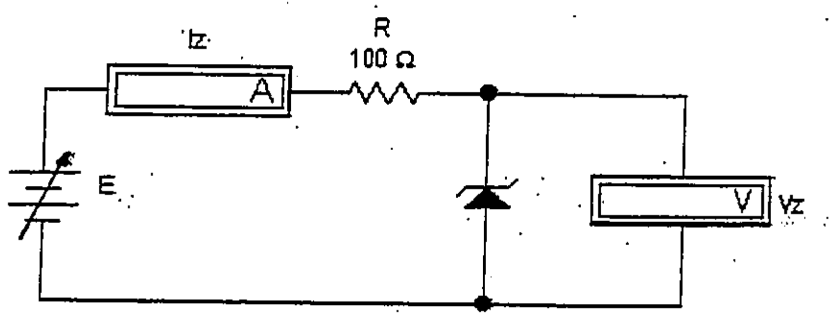


Figure 4.1

2- Apply power to the circuit, increase the voltage E until Vz equals 1v measure Iz, and record its value in Table (4.1).

3- Repeat for the other values of Vz as indicated in Table (4.1), measure and record as you did in step 2.

Zener	Zener

Table 4.1

PART B (ZENER DIODE REGULATOR)

(With Varying Source &Constant Load Resistance)
Procedure:

1- Construct the zener diode regulator circuit of Figure (4.2), set the resistance box to 1 kΩ.

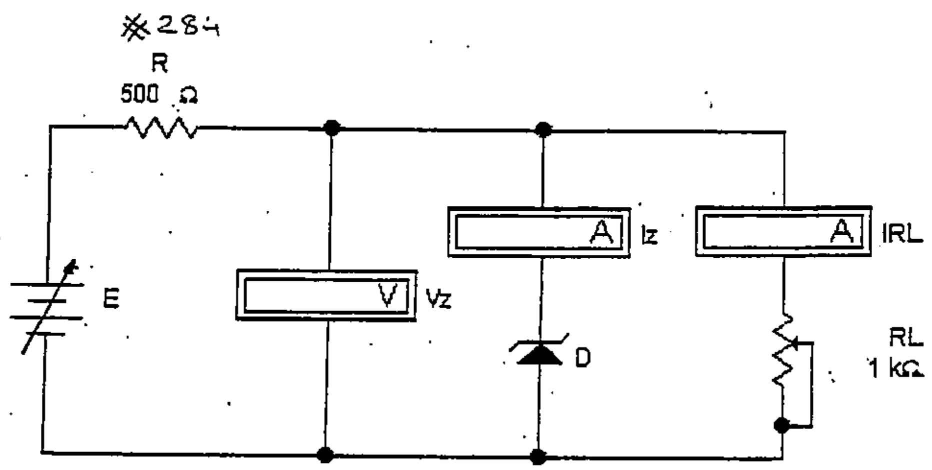


Figure 4.2

2- Increase the voltage as indicated in Table (4.2), measure Vz, Iz, IL and record in the proper spacing.

E (v)	0	2	4	6	8	10	12	14	16	18	20
Vz (v)											
Iz (mA)											
IL (mA)											

Table 4.2

3- We know Vz from part (A), otherwise ask your instructor. Calculate the value of E at which the zener diode should be on using the equation.

$$E = V_{Z(ON)} \frac{R + R_L}{R_L} \longrightarrow$$

(With Varying load &Constant input Source)

4- With the same circuit of Figure (4.2), hold the input voltage constant at 18.5 v.
5- Increase the resistance of resistance box as indicated in Table (4.3), measure and record Vz, Iz, and IL in the proper spacing.

Resistance box (RL)	100Ω	300Ω	500Ω	700Ω	900Ω	1000Ω	1200Ω
Vz							
Iz							
IL							

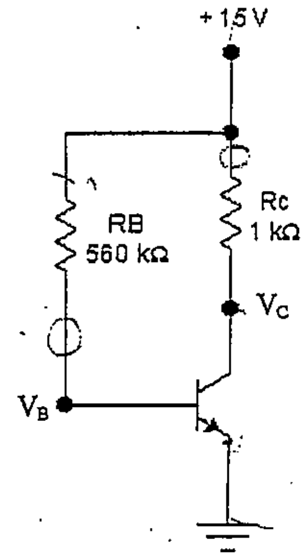
Table 4.3

REPORT:
1- Plot the data in Table 4.1
2-Calculate the right value of RL so that the zener diode will be on.(use voltage divider rule).
3- What is the limitation of zener diode regulator circuit?
4- Write brief conclusion about the main idea of the regulator part of the experiment?

Part I (Experimental)

Procedure:

1- Connect the circuit shown in Figure 5.1.



Note start table 5.2 then 5.1.

Figure 5.1

2- With your AVO-meter, measure the currents through the base and collector resistors, record your values in Table 5.1. From these two sets of values, determine the dc current gain, or beta (β_{dc}), record in Table 5.1.

3- Measure V_B and V_{CEQ}. Record in Table 5.1.

4- Now carefully place a soldering iron near the transistor for a few seconds while measuring the collector current using your AVO-meter. Does the collector increase or decrease?

5- Disconnect power from the circuit and replace the 560-kΩ resistor (R_B) with a 1-MΩ potentiometer. Again apply power to the circuit and connect a voltmeter between the transistor's collector terminal and ground.

6- Now vary the resistance of the potentiometer until V_{CE} as read by the voltmeter reaches a minimum value, $V_{CE(sat)}$. Then measure the corresponding collector current, $I_{C(sat)}$. Record both values in Table 5.2.

7- Continue to vary the resistance of the 1-MΩ potentiometer until V_{CE} reaches a maximum value, $V_{CE(off)}$. Then measure the corresponding collector current $I_{C(off)}$, record both values in Table 5.2.

8- Vary the potentiometer so that you are able to measure about five combinations of I_C and V_{CE} over the active region of the dc load line, recording all values in Table 5.2.

Experiment No. (5)
Transistor Self-Biasing

Objectives:

To study the transistor three states: Saturation, active and cutoff.
To study the effect of β and temperature on transistor's Q-point under active state.

Theoretical Background:

Self-bias is the simplest of the transistor biasing circuit. It consists of single transistor, two resistors, and a power supply.

It would seem that the simplicity of the self-bias circuit would make it ideal for most applications. However, the self-bias circuit is relatively unstable. That is, the Q-point of the circuit will shift (change) if there is a significant change in β and/or temperature. This point will be demonstrated in this experiment. The following equations could be a great help to be able to calculate:

$$V_B = V_{CC} - I_{BQ}R_B = V_{BE}$$

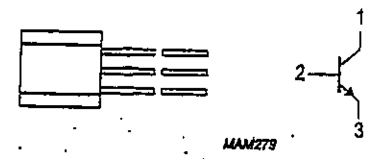
$$I_{CQ} \approx \frac{V_{CC} - V_{BE}}{R_B/\beta}$$

$$I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B}$$

$$V_{CEQ} = V_{CC} - I_{CQ}(R_C)$$

PINNING

PIN	DESCRIPTION
1	collector
2.	base
3	emitter



Simplified outline (TO-92; SOT54) and symbol.

For the dc load line

$$I_{C(Sat)} \cong \frac{V_{CC}}{R_C} \qquad \text{(Saturation)}$$

$$V_{CE(off)} = V_{CC} \qquad \text{(Cutoff)}$$

And β can be calculated by

$$\beta_{dc} = \frac{I_{CQ}}{I_{BQ}}$$

Materials and Equipment:

1- Power supply.
1- AVO meter or digital multi-meter.
1- Transistor npn (# 568 or 571).
1- Resistor, 1 k ohm.
1- Resistor, 560 ohm.
1- Potentiometer, ~~1 M ohm.~~

Part II (calculation)

1- Calculate the values of I_{BQ} and I_{CQ} record in Table 5.1.
2- Calculate the value of V_{CEQ} record in Table 5.1.
3- Calculate the saturation and cutoff on dc load line record in Table 5.2.

Note use β measured for Calculati

Parameter	Measured Value	Calculated Value
I_{BQ}	.026mA	
I_{CQ}	3.5mA	
β_{dc} =		
V_B	0.7	0.7
V_{CEQ}	11.5V	

$I_C = \beta I_B$

$V_{CE} = V_{CC} - I_C R$

Table 5.1

Condition	Calculated Value		Measured Value	
	I_C	V_{CE}	I_C	V_{CE}
Saturation (Step 6)	15V	0		
Cutoff (Step 7)	0	15V		
Active Region (Step 8)	1.5mA	13.5V		
	3	12		
	6	9		
	8	7		
	9	6		

RB

Table 5.2

Report:

1- Plot the calculated point of Table 5.2 on a graph paper.
2- Draw the dc load line, and locate saturation and cutoff.
3- To what extend the measured and the calculated value are identical.
4- Explain the effect of heating the transistor on Q-point and β.
5- Writebrief conclusions about what you have learned form this experiment.

Experiment No. (6)
BJT Biasing (Voltage-Divider Bias)

Objective:

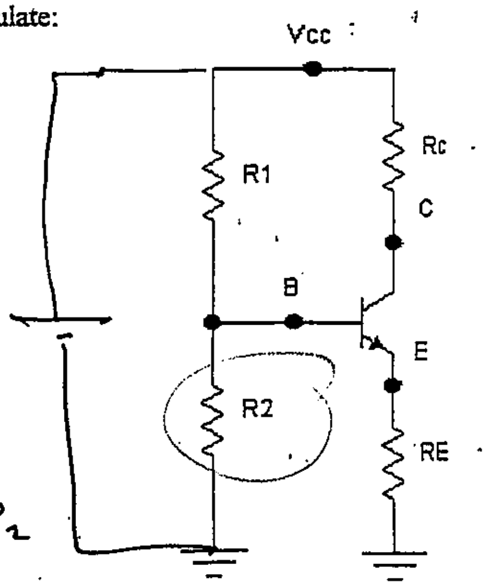
To demonstrate the operation of the voltage-divider bias circuit, and the Q-point stability.

Theoretical Background:

The voltage-divider bias circuit is the most commonly used of the BJT biasing circuit for several reasons:

1- It provides excellent operating point stability even with wide change in β and temperature.
2- It requires only one power supply voltage.
3- It provides a degree of stability with respect to change in supply voltage.

The following equations could be a great help to be able to calculate:



$$V_B = Vcc\frac{R2}{R1+R2}$$

$$V_E = V_B - V_{BE}$$

$$I_E = \frac{VE}{RE}$$

$$I_{CQ} \cong I_E$$

$$V_{CEQ} = Vcc - I_E\,(Rc + R_E)$$

Materials and Equipment:

1-Power supply.
1-AVO-meter (analog).
1-Digital multi-meter.
2-Transistor npn (# 568 or 571)
1- Resistor 560 Ω
1-Resistor 1.5 kΩ
1-Resistor 6.8 kΩ
1-Resistor 33 kΩ
1-Potentiometer 25 kΩ

Part I (Experimental)
Procedure:

1- Set the potentiometer to 18 kΩ (use AVO-meter).

2- Construct the circuit of Figure (6.1).

3- Now apply 12 volts to the circuit, measure and record the points indicated in Table 6.1

4- Adjust Ra until V_B is approximately equals the value calculated in part III step 1, repeat the measurements instep (3).

Ra=18Kω

	Calculation	VB sol
V_B	3.2	1.8
V_E	2.59	1.15
V_{BE}	0.7	0.668
V_C	5.07	9.5
V_{CE}	2.48	8.39
I_E	4.6mA	2 mA

9 8.39

- $V_B = \dfrac{R_2}{R_2 + R_1} V_{CE} = \dfrac{6.8}{18 + 6.8} 12 = 3.2$

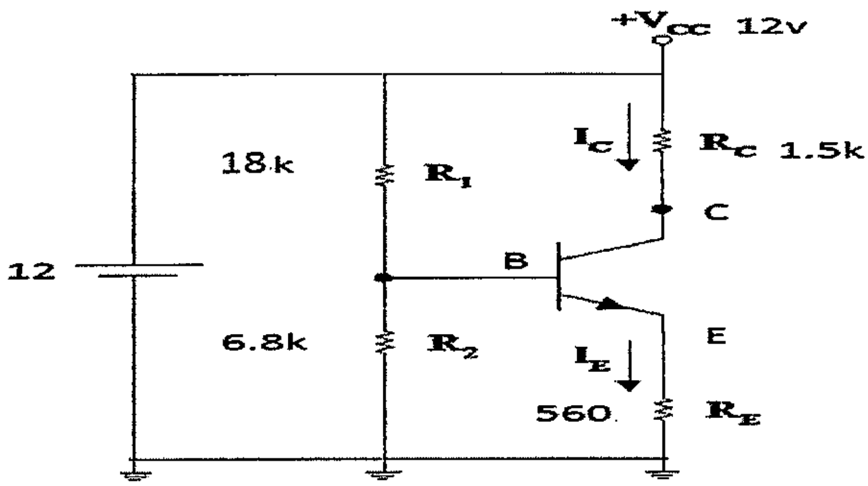
  $I_C R_C = 4.5 \; x \; 1.5$

  $= 6.93$

  for $I_C \approx I_E$

  $- V_{cc} + I_C R_C + V_C = 0$

  $V_C = 5.07$

- 

	Calculation
V_B	1.9
V_E	1.2
V_{BE}	0.7
V_C	9
V_{CE}	7.8
I_E	2 mA

- $$V_B = \frac{R_2}{R_2 + R_1} V_{CE} = \frac{6.8}{36 + 6.8} 12 = 1.9$$

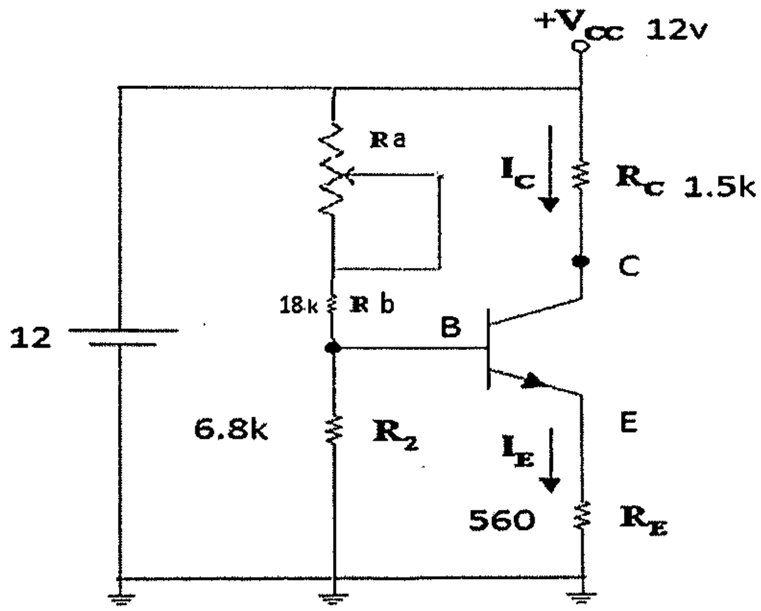
$I_C R_C = 2 x 1.5$

$= 3$

for $I_C \approx I_E$

$-V_{cc} + I_C R_C + V_C = 0$

$V_C = 9$



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يتم تغير المقاومة حتى يصبح قيمة V B=1.9

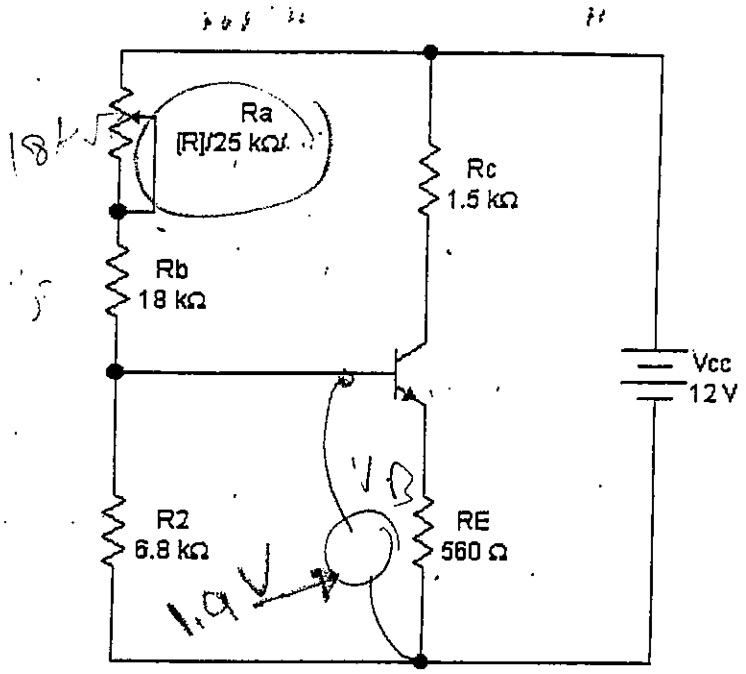


Figure 6.1

Measurements	Computer Simulation	Experimental		Calculation
		R_a=18 k	V_B (set) 1.9 V	
V_B				1.9
V_E				
V_{BE}				
V_C				
V_{CE}				
I_E				

Table 6.1

Part II (Computer Simulation)
Procedure:

1- Setup the circuit of Figure 6.1 using (Electronics Workbench Software).
2- Setup R_a to 18 kΩ.
3- Measure the points indicated in Table 6.1 and record under computer simulation column.

Part III (Calculation)
Procedure:

1- With R_4 equals 18 kΩ, calculate V_B.
2- Calculate I_B, and I_C.
3- Calculate the rest of the points, record in Table 6.1 under calculation column.

Report:

1- Compare between the columns of measurement, verify the changes if there is any.
2- Write brief conclusion about the advantages of the circuit.

$$V_B = V_{cc} \frac{R_2}{R_1 + R_2}$$

$$V_E = V_B - V_{BE} = 3.2 - 0.7$$

$$V_{CE} = V_{cc}$$

$$-12 + I_C R_C + V_{CE} + I_E R_E = 0$$

$$12 - 6.93 - (4.6 \times 560) = V_{CE}$$

2.576

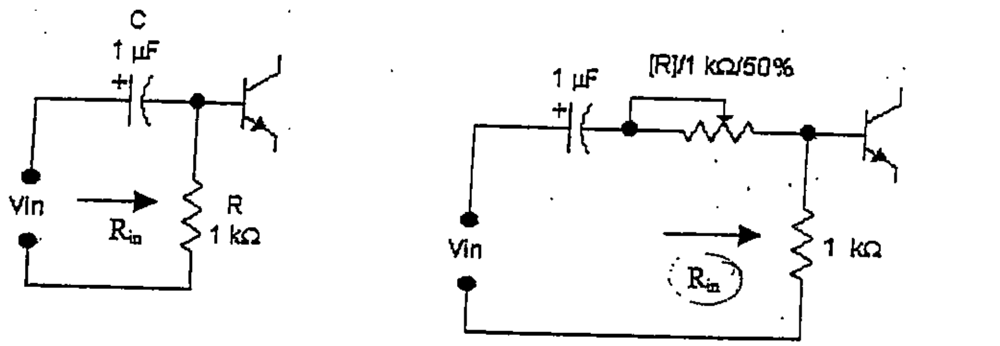
Experiment No. (7)
Impedance, Power, and Phase Relationship of A Common-Emitter Amplifier

Objectives:

To be come familiar with the measure of power gain, input and output impedance and investigate the phase relationship between the output and input signals of a common-emitter amplifier.

Theoretical Background:

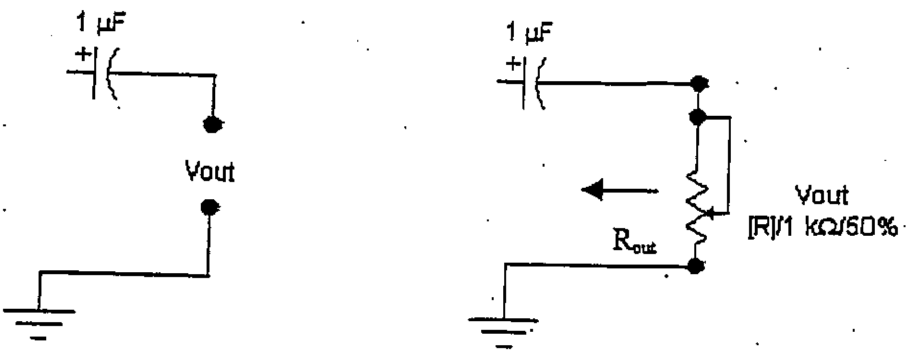
The common-(ground)-emitter amplifier has been described as a power amplifier. Power can be computed from the equation $P = V^2/R$. The input power of CE amplifier is $P_{IN} = V^2_{IN}/R_{IN}$. The output power is $P_{out} = V^2_{out}/R_{out}$ To determine R_{IN} and R_{OUT}. A method for determining R_{IN} is shown in Figure 7.1. Figure 7.1(a) shows the standard input circuit, Figure 7.1(b) we have added a variable resistance (potentiometer).



(a) (b)

Figure 7.1

First, we set the potentiometer to zero and adjust V_{IN} until we have an easily measured value of V_{OUT}. Then we adjust the potentiometer until the output voltage is exactly one-half. We have a voltage divider on the input. Half the voltage is dropped across the potentiometer. The other half is dropped across R_{IN}. Therefor, R_{IN} must be equal to the resistance value we have set on the potentiometer. We then remove the potentiometer from the circuit and measure its value with an ohmmeter. This gives us the value of R_{IN}.
A similar thing is done to measure R_{OUT}.



(a) (b)

Fig 7.2

Again we have a voltage divider made up of R_{OUT} and the potentiometer. First, without the potentiometer Fig 7.2 (a), we set the output to some value, then we put the potentiometer across the output as shown in Fig 7.2 (b) and adjust its resistance until the output is exactly is one-half that previously measured. Again remove the
potentiometer from the circuit and measure its resistance, this is the output impedance R_{OUT}.
Power gain given by the equation: $P = P_{OUT} / P_{IN}$. This can be computed by substituting V^2/I for P.
Rather than express power gain as the absolute ratio of P_{OUT} to P_{IN}, it is usually expressed in decibels.
Power gain in decibels = 10 log (P_{OUT} / P_{IN}).
In a CE amplifier, the output signal voltage is 180° out of phase with the input signal voltage at the base. This relationship is easy to keep in mind when we remember how transistors perform a switching function. With 0 input at the base, the transistor does not conduct. Therefore, virtually the entire V_{CC} appears across the output. When a signal is put on the base so as to drive the transistor into saturation, it conducts for the full cycle and the voltage across it is zero.

Materials and Equipment:

1 DC power supply
1 AF signal generator
1 Oscilloscope
1 AVO meter
1 Resistor, 560 ohm
1 Resistor, 1k ohm
1 Resistor, 8.2k ohm
1 Resistor, 18k ohm
1 Capacitor, 100 µF
2 Capacitors, 25 µF
1 Transistor, 2N3904(# 571)
1 Potentiometer, 1k ohm
1 Potentiometer, 5k ohm
1 Computer (with Electronic Workbench software)

PART I (Experimental)

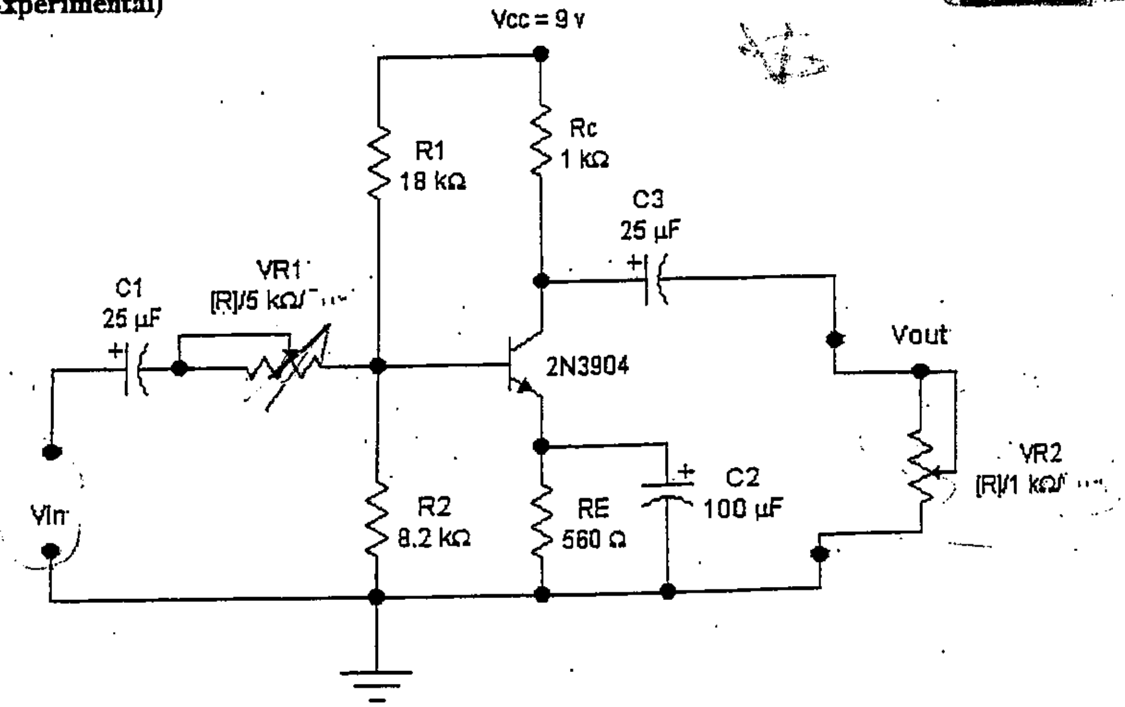


Figure 7.3

Procedure:

1- a) Connect the circuit of Figure 7.3.

b) Measure I_C, I_E, and I_B, record to be used in the calculation part.

2- a) Set the 5k Ω potentiometer to **zero** ohms.

b) Set the signal generator for 1 kHz and apply its output to V_{IN}.

c) Set the oscilloscope to view V_{OUT}.

3- Turn ON the power and adjust the output signal generator until V_{OUT} reads 6 volts peak-to-peak on the oscilloscope.

4- Increase the resistance of the potentiometer until the output voltage is exactly 3 volts peak-to-peak.

5- a) Turn off the power and the signal generator.

b) Remove the potentiometer from the circuit and without changing its setting, measure its resistance.

c) Record this as R_{IN} in Table 7.1.

6- a) Put a lead in the circuit in place of the input potentiometer.

b) Turn ON the signal generator.

c) Repeat step 3.

7- Connect the 1 kΩ potentiometer across the output terminals, as shown in Fig 7.3.

8- Adjust the potentiometer until the output voltage is exactly 3 volts peak-to-peak.

9- a) Turn OFF the power and the signal generator.

b) Remove the potentiometer from the circuit and without changing its setting, measure its resistance.

c) Record this as R_{OUT} in Table 7.1.

10-Turn ON the power, with the signal generator still set to 1 kHz, adjust its output until the output voltage of the amplifier reads 6 volts peak-to-peak.

11-Measure the input voltage (peak-to-peak) and record the value of V_{IN} in Table 7.1.

12- a) With the same setting as in step 11 connect a load resistor of 1kΩ across the output terminal.

b) Measure the output voltage (V_O) w/L record in Table 7.1.

... input and output signals.

PART II (Computer Simulation)

Procedure:

1- Set up the circuit of Figure 7.3 using (Electronics Workbench Software).

2- Go through the same procedure as you did in your experimental part from step 2 to step 11.

3- Under analysis Menu go for AC frequency analysis.

4- Select 1Hz as start frequency and 10 GHz as end frequency, do not [illegible] to select the proper nodes the input and the output.

5- Observe the frequency response and the phase angle, record in Table 7.1.

Measurements	Computer Simulation	Experimental	Calculation
Input Impedance R_{IN} (ohms)			
Output Impedance R_{OUT} (ohms)			
Input Voltage V_{IN} (p-p)			
Output Voltage V_{OUT} (p-p)			
Output Voltage V_{OUT}(p-p)$_{w/L}$			
Voltage Gain A_V			
Voltage Gain $A_{Vw/L}$			
Power Gain A_P			
Power Gain (dB) PG_{dB}			
Phase angle (degree)			

Table 7.1

PART III (Calculation)

1- Use the measured data in step 1 (b) in the experimental part to calculate β, and r_e.
2- Draw the equivalent ac model.
3- Calculate the input and output impedance R_{IN}, and R_{OUT}.
4- Calculate the voltage gain A_V, and the current gain A_i.

REPORT:

1- Compare between the data in the three columns in Table 7.1.
2- Under data analysis in your report, write your opinion about step 1 of the report section.
3- Write what you have concluded from this experiment.

Experiment No. (8)
The Emitter Follower

Objective:

To become familiar with the common-collector amplifier, also known as emitter follower.

Theoretical Background:

The common-emitter amplifier had voltage, current and power gain. The common-collector amplifier, on the other hand, has only current and power gain. The voltage gain is a little less than 1. The common-collector amplifier has high input impedance and low output impedance, however, making it ideal for impedance matching applications, known as buffer stage.

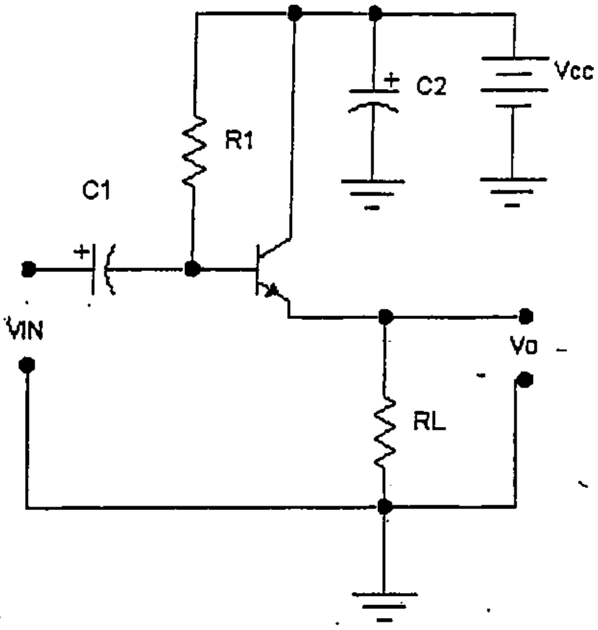


Fig 8.1

Figure 8.1 shows a common-emitter amplifier, the input signal V_{IN}, is coupled to the base through capacitor C_1. The load resistor, across which V_O is taken, is connected to the emitter. Note that the collector is at AC ground because capacitor C_2 acts as a low-impedance AC path. The collector is connected directly to V_{CC}. The input signal, V_{IN}, appears between base and ground (collector), and the output signal appears between emitter and ground (collector). This makes the collector common to both input and output.

Consider what happens when V_{IN} increases during a positive AC alternation. Both the collector current and the emitter current increase. Emitter voltage $V_O = I_E R_L$, therefore, becomes more positive. In other words, when V_{IN} goes positive, V_O (emitter voltage) follows. This is why this amplifier is called an emitter follower. Note that **V_O is in phase with V_{IN}.**

The base current, I_B, is amplified by a factor of β. Output current, then is βI_B. We can look upon this as two loop that have R_L as a common leg and write Kirchhoff's voltage law equation. One loop (neglecting C_1) is made up of the source, V_{IN}; the base-to-emitter resistance, R_B, 9through which I_B flows) and the resistance, R_L (through which $I_B + \beta I_B$ flows). Therefore,

$$V_{IN} = I_B R_B + I_B R_L + \beta I_B R_L$$

$$V_{IN} = I_B (R_B + I_B R_L + \beta R_L)$$

$$V_{IN} = I_B (R_B + R_L (\beta+1))$$

New, let's look at the second loop, make up the output voltage, V_O, and the resistance, R_L, (through which $I_B+\beta I_B$ flows):

$$V_O = I_B R_L + \beta I_B R_L$$

$$V_O = I_B R_L (\beta+1)$$

We can, therefore, substitute in the equation for voltage gain, $A_V = V_O / V_{IN}$.

$$A_V = \frac{I_B R_L (\beta+1)}{I_B (R_B + R_L (\beta+1))}$$ The I_B 's cancel

$$A_V = \frac{R_L (\beta+1)}{R_B + R_L (\beta+1)}$$

For example, assume the following values: $\beta = 99$; $R_L = 1000$ ohms, $R_B = 2000$ ohms.

$$A_V = \frac{1000 \times (99 + 1)}{2000 + 1000 \times (99+1)} = 0.98$$

Without R_L, V_{IN} would be simply $I_B R_B$. We saw, however, that the effective value of the input impedance was increased with the addition of R_L. In fact, it becomes $R_B + R_L (\beta+1)$. In our example, instead of 2000 ohms, the input impedance was a 102000 ohms.

Since the phase of signal voltage (emitter-to-ground) is the same as the base voltage (base-to-ground), and since the input signal voltage to the circuit is the difference between the base voltage and emitter voltage, the effect of the un-bypassed emitter resistor is to provide degenerative, or negative, feedback to the circuit. In other words, the amplifier sees a lower effective input signal between base and emitter than V_{IN}.

Materials equipment:

1 DC Power Supply
1 AF Signal Generator
1 Oscilloscope
1 AVO meter
1 Resistor, 1 k ohms
1 Resistor, 470 k ohms
1 Capacitor, 25 μF
1 Capacitor, 100 μF
1 Transistor, 2N2102
1 Potentiometer, 1 k ohm
1 Potentiometer, 500 k ohm

Part I (Experimental)
Procedure:

1- Connect the circuit of Figure 8.2 with R_{V1} set to zero ohms.

2- Measure I_B and I_C, to be used in part III (calculation).

3- a- Set the Signal Generator for 1000 Hz.

b- Apply power to the circuit.

c- Connect the output of the Signal Generator to the input of the circuit, with no load (R_{V2} disconnected).

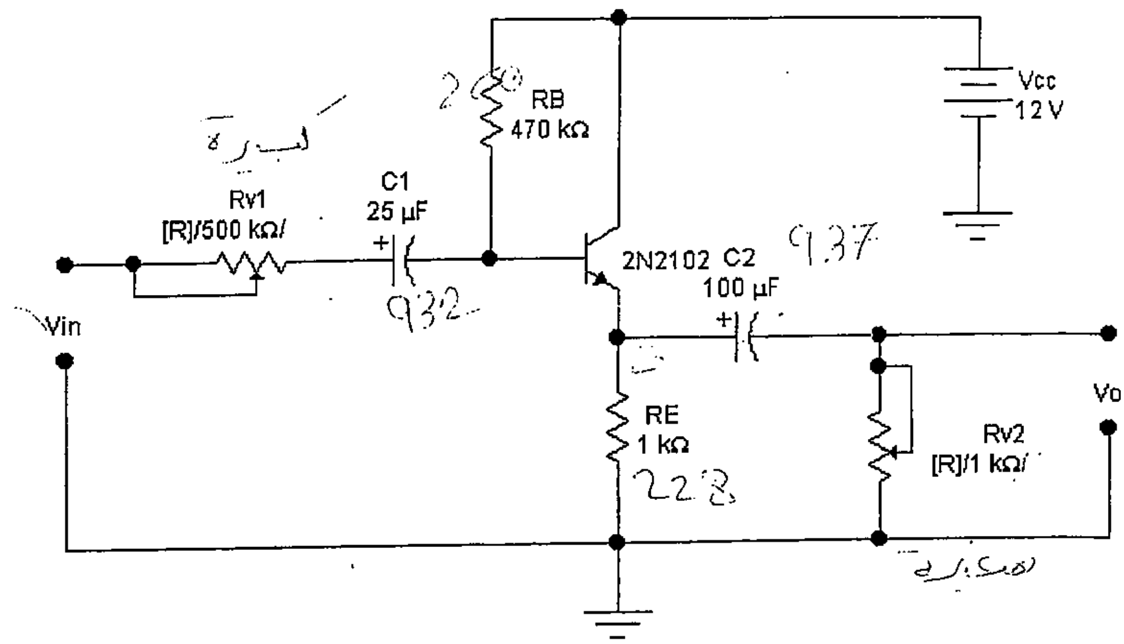


Fig 8.2

4- a- Connect the Oscilloscope to the output terminals to observe V_O.

b- Set the Signal Generator to a value that produces an undistorted output waveform measuring **150 V peak-to-peak.**

5- Measure the peak-to-peak value of V_{IN} and record in Table 8.1.

6- Adjust the 500-k ohm potentiometer until the output waveform measures exactly 75 mV peak-to-pea

7- a-Switch off the power.

b- Disconnect the potentiometer from the circuit.

c- Measure its resistance and record as R_{IN} in Table 8.1.

8- a- Replace the 500 k ohm potentiometer by a wire.

b- Repeat step 3.

c- Connect the 1 k ohm potentiometer in parallel with the output.

d- Adjust it until the output measures exactly 75 m V peak-to-peak.

e- Disconnect from the circuit, measure its value and record as R_{OUT} in Table 8.1

(ترونب)

CC :

* common collector $AV \leq 1$

collector common bet I & O

ف Ac model ——→ collector ——→ موصل بالبطارية

في Ac model تصير جراوند

I ناخذه من B

لأن

فهو مشترك

لأن O ناخذه من E

المشترك C بين O & I

We can't use as voltage amplifier

but we can use as current amp

because $A_V \leq 1$ $V_0 = V_i$

---

we use it in impedance matching application

يربط بين دائرتين

Ac ——→ capacitor ——→ ~~scho~~ short circuit

9- Use your measurements, calculate voltage gain A_V, input power, and output power record in Table8.1.

10- Using the data in step 9 calculate the power gain A_P.

Vi = 150mV
Vo = 150mV
Ri = 51 K
Ro = 22.4Ω

Part II (Computer Simulation)

Procedure:

1- Set up the circuit of Figure 8.2 using **(Electronics Workbench Software)**, make shore that the 500-k ohm potentiometer is set to zero ohm.
2- Go through the same procedure as you did in your experimental part from step 3 to step 10.
3- Under Analysis menu go for AC frequency analysis, select **1 Hz** as start frequency and **10 GHz** as end frequency, do not forget to select the proper nodes (the input and the output).
4- Observe the frequency response and the phase angle, record in Table 8.1.

2V / 2V

Measurements	Computer Simulation	Experimental	Calculation
Output voltage (V_O)	**150 mV_{P-P}**	**150 mV_{P-P}**	
Input voltage (V_{IN})	150mV		
Voltage gain (A_V)	1		Vo/Vi
Input impedance (R_{IN})	160K → 200K	60K Ω	
Output impedance (R_{OUT})	40 Ω	400 Ω	
Input power (P_{IN}) = V^2_{IN} / R_{IN}	1.406×10^{-7}		
Output power (P_{OUT}) = V^2_{OUT} / R_{OUT}	.0005625		
Power gain (A_P) = P_{OUT} / P_{IN}	4000.7		

Table 8.1

Part III (Calculation)

1- Using the measured data in step 2 in the experimental part to calculate β, and re.
2- Draw the equivalent ac model.
3- Calculate the input and output impedance R_{IN}, and R_{OUT}.
4- Calculate the voltage gain A_V, and the current gain A_i.

REPORT:

1- To how extend computer simulation, experimental, and calculation results are identical.
2- Write what you have concluded from this experiment.

$B = \frac{I_C}{I_B}$ $r_e = \frac{26mV}{I_{E\ measured}}$

$Z_i = R_B // B(r_e + R_E)$ (R_B → 470KΩ, R_E → 1KΩ)

$A_V = \frac{R_E}{r_e + R_E} \approx 1$

$A_I = \frac{-B R_B}{R_B + B(r_e + R_E)}$

$Z_o = r_e // R_E \approx r_e$

$B = \frac{I_C}{I_B}$

$r_e = \frac{26mV}{I_E}$

$I_E = 1.16mA$ $I_C = 1.14mA$ $I_B = .02mA$

$B = \frac{I_C}{I_B} = \frac{1.14}{.02} = 57$

$r_e = \frac{26mV}{1.16mA} = 22.4$ ← R_O

$Z_i = 470K // 57(22.4 + 1000)$

470K // 58 $\frac{470 \times 58}{\ }$ = 27260 = 51KΩ

(اكرونت)

CC :

* common collector $A_V \leq 1$

collector common bet I & O

في Ac model ⟶ collector ⟶ موصل بالبطاريه

في Ac model تصير جراوند

لأن هو مشترك

I ناخذه من B

لأن O ناخذه من E

المشترك C بين O & I

We can't use as voltage amplifier
but we can use as current amp
because $A_V \leq 1$ $V_O = V_i$

---

we use it in impedance matching application

يربط بين دائرتين

Ac ⟶ capacitor ⟶ ~~seho~~ short circuit

3- a- Set the Signal Generator for 1000 Hz.

b- Apply power to the circuit.

c- Connect the output of the Signal Generator to the input of the circuit, with no load (R_{V2} disconnected).

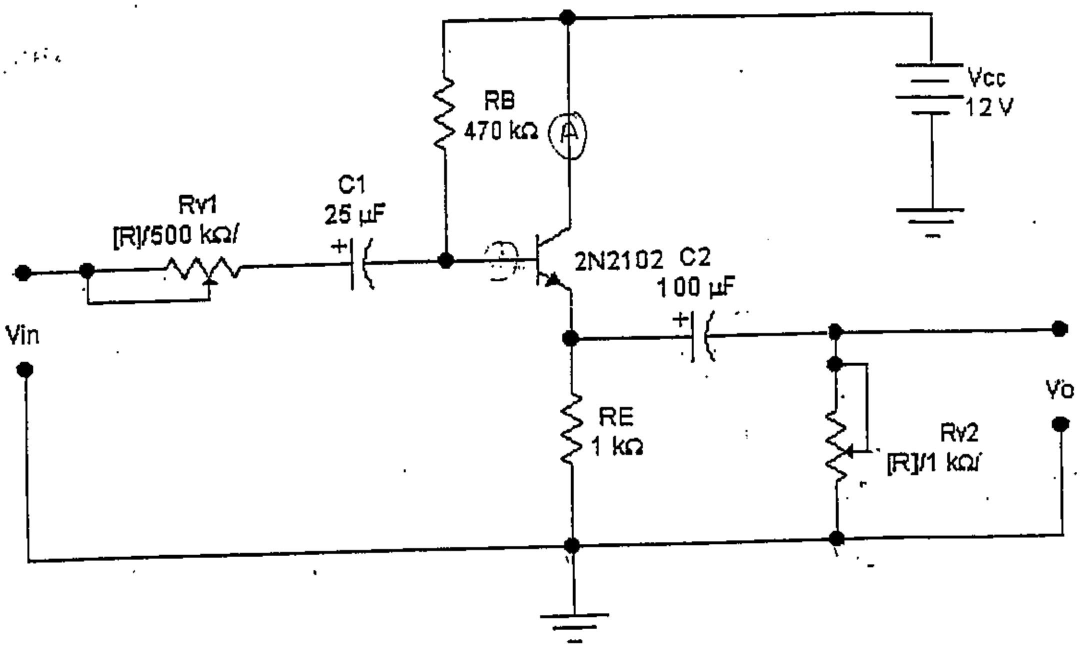


Fig 8.2

4- a- Connect the Oscilloscope to the output terminals to observe V_O.

b- Set the Signal Generator to a value that produces an undistorted output waveform measuring **<u>150 m V</u> peak-to-peak.**

5- Measure the peak-to-peak value of V_{IN} and record in Table 8.1.

6- Adjust the 500-k ohm potentiometer until the output waveform measures exactly 75 mV peak-to-peak.

7- a-Switch off the power.

b- Disconnect the potentiometer from the circuit.

c- Measure its resistance and record as R_{IN} in Table 8.1.

8- a- Replace the 500 k ohm potentiometer by a wire.

b- Repeat step 3.

c- Connect the 1 k ohm potentiometer in parallel with the output.

d- Adjust it until the output measures exactly 75 m V peak-to-peak.

e- Disconnect from the circuit, measure its value and record as R_{OUT} in Table 8.1

9- Use your measurements, calculate voltage gain A_V, input power, and output power record in Table8.1.

10- Using the data in step 9 calculate the power gain A_P.

Part II (Computer Simulation)

Procedure:

1- Set up the circuit of Figure 8.2 using (**Electronics Workbench Software**), make shore that the 500-k ohm potentiometer is set to zero ohm.
2- Go through the same procedure as you did in your experimental part from step 3 to step 10.
3- Under Analysis menu go for AC frequency analysis, select 1 Hz as start frequency and 10 GHz as end frequency, do not forget to select the proper nodes (the input and the output).
4- Observe the frequency response and the phase angle, record in Table 8.1.

Measurements	Computer Simulation	Experimental	Calculation
Output voltage (V_O)	150 mV_{P-P}	150 mV_{P-P}	
Input voltage (V_{IN})			
Voltage gain (A_V)			
Input impedance (R_{IN})			
Output impedance (R_{OUT})			
Input power (P_{IN}) = V^2_{IN} / R_{IN}			
Output power (P_{OUT}) = V^2_{OUT} / R_{OUT}			
Power gain (A_P) = P_{OUT} / P_{IN}			

Table 8.1

Part III (Calculation)

1- Using the measured data in step 2 in the experimental part to calculate β, and re.
2- Draw the equivalent ac model.
3- Calculate the input and output impedance R_{IN}, and R_{OUT}.
4- Calculate the voltage gain A_V, and the current gain A_i.

REPORT:

1- To how extend computer simulation, experimental, and calculation results are identical.
2- Write what you have concluded from this experiment.

Experiment No. (9)
JFET Common-Source Amplifier

Objective:

To gain an understanding of the JFET common-source amplifier.

Theoretical Background:

The common-source amplifier, which we have been using, is the most common type of JFET amplifier. It is also called a ground-source amplifier because the source end of the circuit is common to both the input and output and is at the lowest voltage of any point in the circuit.

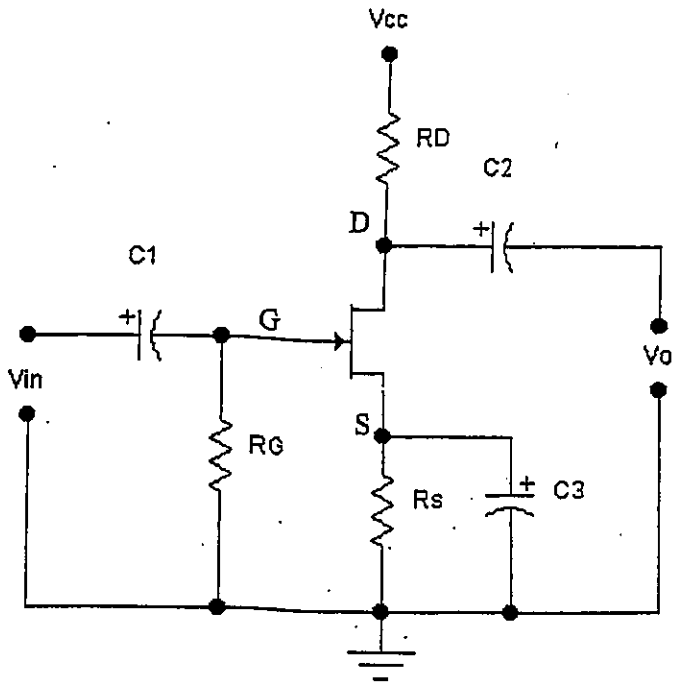


Figure 9.1

Figure 9.1 shows a common-source amplifier. To isolate the gate from the source, the input signal, V_{in} is coupled to gate through capacitor C_1. The value of the capacitor is chosen to present a very low reactance to signals in the frequency range over which it is to operate.

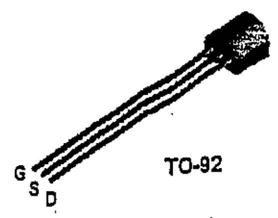
A load resistor in series with the drain R_D, provides a means of limiting drain-to-source voltage to a pre-Determined value. The gate resistor is usually quite large. The exact value isn't important, as long as it is large enough not to short out the input signal. Its purpose is to tie the gate to ground. Since no current flows in the gate circuit as long as the gate is negative ($-V_{GS}$) there is no voltage drop across R_G. one end of it has the same DC potential as the other.

Current does flow through R_S, however from the positive terminal of the supply, through R_D, through the JFET, through R_S and back to the negative terminal. That makes the top end of R_S more positive than the bottom end. Since the gate is effectively connected to the bottom end of R_S, the gate is more negative than the source. This is just what we need for a negative bias on JFET gate.

The common-source amplifier has high input impedance, high output impedance, and good voltage gain.

Materials and Equipment:

2N5459



N-Channel General Purpose Amplifier

1- DC Power supply.
1- AF Signal Generator.
1- AVO meter.
1- N-channel JFET 2N5459.
1- Resistor, 390 ohm.
1- Resistor, 390 ohm.
1- Potentiometer, 1 k ohm.
2- Capacitor, 0.05 μF.
1- Capacitor, 25 μF.

Part I (Experimental)
Procedure:

1- Identify the JFET terminals.

2- Connect the circuit of Figure 9.2.

3- Set R_S initially to 300 Ω, to measure the value of g_m for a JFET.

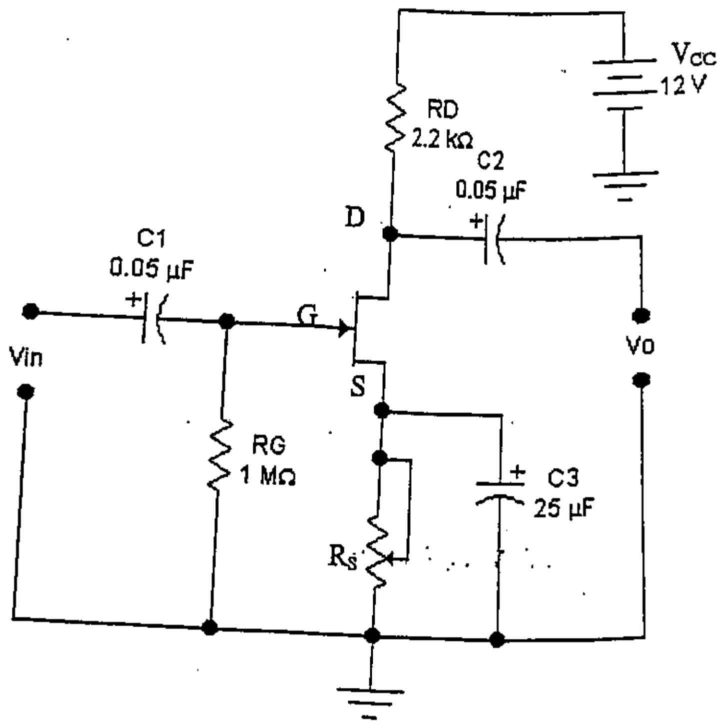


Figure 9.2

4- With R_S set to 300 Ω, measure V_{GS}, I_D and record in Table 9.1.

5- Adjust R_S to a value of 400 Ω, and measure V_{GS}, I_D again and record in Table 9.1.

6- Using your data calculate the amplifier gain A_V

$$A_V = g_m R_D$$

**********	Experimental R_S		Computer Simulation R_S	
Measurement	300 Ω	400 Ω	300 Ω	400 Ω
V_{GS}				
I_D				

Table 9.1

7- Switch the power off, replace the 1 kΩ potentiometer with 390 Ω fixed resistor.

8- With the AVO meter, measure and record in Table 8.2 the **DC** drain-to-ground voltage, V_D.

9- Measure and record in Table 9.1 the **DC** voltage drop across the 390 Ω source resistor, V_{RG}.

10- Measure and record in Table 9.1 the **DC** bias voltage from gate-to source, V_{GS}.

11- Turn on the signal generator and set it for 1000 Hz at 1 volt peak-to-peak.

12-Measure the peak-to-peak value of the output signal V_O, record in Table 9.2.

13-Calculate the amplifier gain using the equation $A_V = V_O/V_{in}$ record your result in Table 9.2.

14- Adjust the vertical sensitivity of your oscilloscope channels so that you can observe both the input and output waveforms on the CTR at the same time. Then neatly draw the two waveforms in their proper phase relationship.

Measurement	Computer Simulation	Experimental	Calculation
V_D(DC)			
V_{RS}(DC)			
V_{GS}(DC)			
V_{in}(p-p)	1 V	1 V	1 V
V_O(p-p)			
GAIN $A_V = V_O/V_{in}$			
GAIN $A_V = g_m R_D$			

Table 9.2

Part II (Computer Simulation)
Procedure:

1- Set up the circuit of Figure 9.2 using (Electronics Workbench Software).

2- Go through the same procedure as you did in the experimental part from step 2 to 14.

3- Under analysis menu go for AC frequency analysis.

4- Select **1 Hz** as start frequency and **100 MHz** as end frequency.

5- Observe the frequency response and the phase angle.

Part III (Calculation)

1- Given I_{DSS} = 6 mA, and V_P = – 3 V, draw the transfer characteristics for the JFET.
2- Determine I_D, and V_{GS}.
3- Draw the equivalent AC model for the circuit of Figure 9.2.
4- Calculate R_{in}, and R_{out}.
5- Calculate I_D, V_D, V_{RS}, V_{GS}, and the gain A_V.

Report:

1- To how extent the columns of Table 9.2 are identical.
2- Under data analysis in your report, write your opinion about step 1.
3- Write what you have concluded from this experiment.

Experiment No. (10)
JFET COMMON-DRAIN AMPLIFIER

Objective:

To investigate the operation of a common-drain JFET amplifier.

Theoretical Background:

The common-drain amplifier is also called a source-follower. In many ways, it is similar to the emitter-follower circuit of the bipolar transistor. Like the common-source, the source follower has high input impedance. Unlike the common-source amplifier, however, its input impedance is relatively low and its voltage gain is always less than 1. It is mainly used as an impedance matching device.

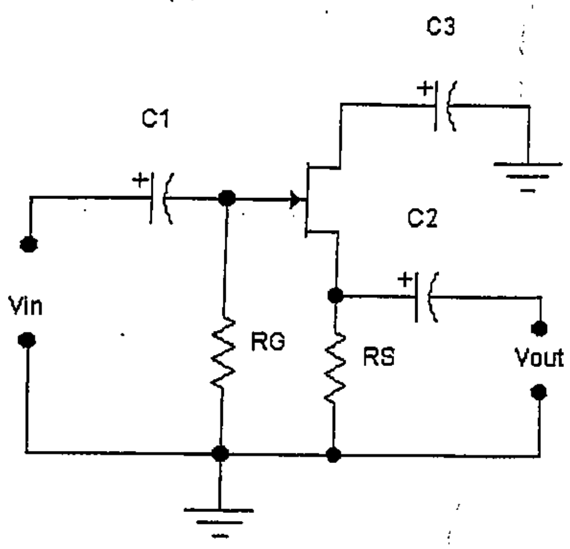


Figure 10.1

In a source-follower amplifier, the output signal appears across R_S as shown in Fig 10.1. Naturally, this means that the bypass capacitor must be eliminated. Going around the loop composed of R_G, the JFET, and R_S, it becomes obvious that:

V_{RS} (the output voltage) = V_{RG} (the input voltage) – V_{GS}

That's why the output voltage, V_O must be less than the input voltage, V_{IN}.
As before, the value of R_S sets the gate bias voltage. It is also true that the higher the value of Rs, the closer the gain approaches 1. Therefore, a voltage divider is used so that R_S can be made larger.

The input impedance if a JFET source-follower amplifier is high. It is kept high value of R_G. The high the resistance, the greater the effect. However, if the gate resistance is returned to the voltage divider instead of to ground, the input impedance looks much higher than R_G to the preceding stage. In fact, what the preceding stage sees is R_G in series with the parallel combination of the two biasing resistors (R_1 and R_2).

Also, looking back from the load, the output impedance is seen much lower than the value of R_S. Since the drain is common, the reciprocal of the transconductance ($1/g_m$) looks like a resistance in parallel with R_S. If you assume a transconductance of 2500 micromohos, the reciprocal is 400 ohms. Assuming R_S = 1000 ohms, the load sees an output impedance of:

$$Z_{OUT} = 1/g_m \,||\, R_S = 400 \,||\, 1000 = 286 \text{ ohms.}$$

Material and Equipment:

1 DC Power Supply
1 AF Signal Generator
1 Oscilloscope
1 AVO meter
1 n-channel, JFET, 2N5459
1 Resistor, 4.7 ohm
1 Resistor, 8.2 ohm
1 Resistor, 10 k ohm
1 Resistor, 33 k ohm
3 Capacitor, 0.05 μF
1 Capacitor, 1 μF

Part I (Experimental)
Procedure:

1- Connect the circuit of Figure 10.2.

2- Apply a 20 volts DC to the circuit.

3- Measure and record in Table 10.1, the DC voltage drop across each of the resistors, the drain-to-source voltage, V_{DS}, and the gate-to-source voltage, V_{GS}, of the JFET.

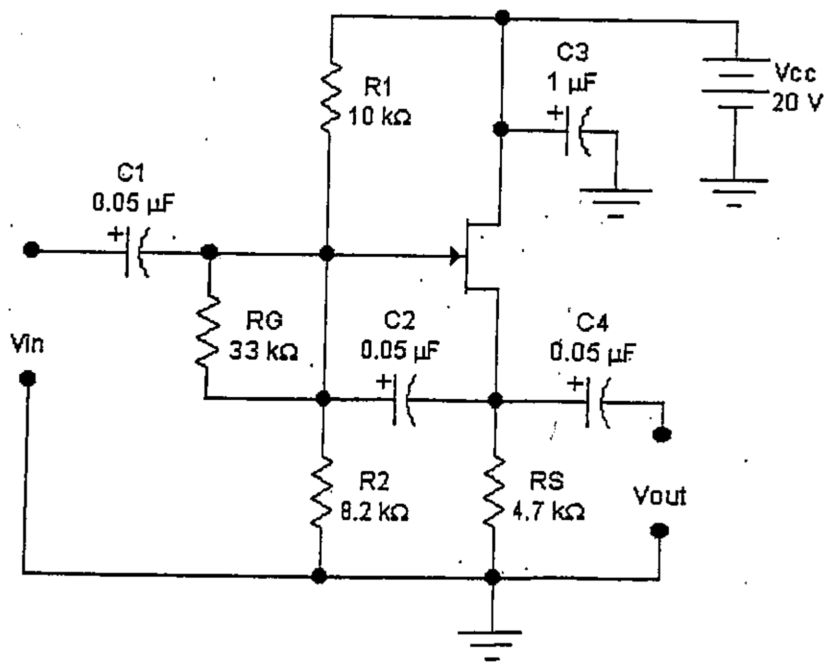


Fig 10.2

4- Set the Signal Generator to 1000 Hz at 1 volt peak-to-peak.

5- Connect the Signal Generator to the input terminals.

6- Measure the peak-to-peak value of the output, V_{OUT}. Record in Table 10.1.

7- Set your Oscilloscope for external triggering. With the scope triggered from the output of the Signal Generator, observe the waveform of the output signal. Record in table 10.1 the degrees that the output signal has shifted from the input signal.

Measurements	Computer Simulation	Experimental	Calculation
V_{R1} (DC)			
V_{R2} (DC)			
V_{RG} (DC)			
V_{RS} (DC)			
V_{DS} (DC)			
V_{GS} (DC)			
V_{IN} (p-p)			
V_{OUT} (p-p)			
Gain $A_V = V_O/V_I$			
Degrees Shift			

Table 10.1

Part II (Computer Simulation)
Procedure:

1- Setup the circuit of Figure 10.2 using (Electronics Workbench Software).

2- Go through the same procedure as you did in the experimental part from set 1 to step 7.

3- Under analysis menu go for AC frequency analysis.

4- Set 1 Hz as start frequency and 1 GHz as end frequency.

5- Observe and record the frequency response and the phase shift.

Part III (Calculation)

1- Given g_m = 2500 micromhos, I_{DSS} = 6 mA and V_P = – 3 V, draw the transfer characteristics for the JFET.
2- Determine I_D, and V_{GS}.
3- Draw the equivalent AC model for the circuit of Figure 10.2.
4- Calculate R_{IN} and R_{OUT}.
5- Calculate V_{R1}, V_{R2}, V_{RG}, V_{RS}, V_{DS}, V_{GS}, and the gain.

Report:

1- Compare between the data in the three columns in Table 10.1.
2- Under data analysis in your report, write your opinion about step 1.
3- Write what you have concluded from this experiment.